DEC-11-HLSAA-A-D

LS11 line printer manual

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FOREWORD

This manual is intended to provide the user with the theory of operation and logic diagrams necessary to understand and maintain the LS11 Line Printer Controller. The level of discussion consists of general and detailed descriptions of the LS11 Controller, as well as line printer information pertinent to LS11 operation. Detailed coverage of the line printer (Centronics 101, 101A, 101D, 102A, or 303) appears in the manufacturer's manual supplied with the line printer.

Although control signals and data are transferred between the LS11 Controller and the Unibus, it is beyond the scope of this manual to cover operation of the bus itself. Detailed Unibus information is contained in the *PDP-11 Peripherals and Interfacing Handbook.*

A copy of this manual is included with each LS11 Controller that is purchased. In various places within this manual, reference is made to engineering drawings. These engineering drawings may be found in the *LS11 Line Printer Controller Engineering Drawings Manual*, also shipped with each LS11 Controller. The engineering drawings manual contains the current, updated LS11 prints as of the time the equipment is shipped.

CHAPTER 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

The LS11 Controller is the interface between a Centronics (Models 101, 101A*, 101D, 102A, or 303) line printer and the Unibus (Figure 1-1). This line printer system can be used with all computers of the PDP-11 family. The LS11 is implemented on a single M7258 quad integrated circuit module. The pin assignments are such that the DD11 small peripheral system unit can be used, permitting four LS11s to be mounted in a single system unit. Because the LS11 Controller conforms to the DD11 wiring scheme, it is considered to be a small peripheral controller (SPC), and conforms to all SPC configuration rules.

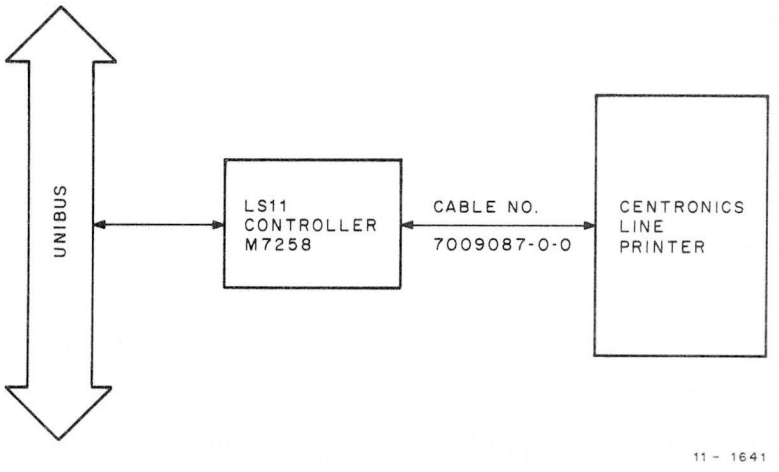


Figure 1-1 LS11 Line Printer System

1.2 FUNCTIONAL DESCRIPTION

Under program control, the PDP-11 processor transfers 7-bit ASCII characters to the LS11 via the Unibus. The LS11, in turn, transfers the characters to the line printer while maintaining program status information and generating program interrupts.

* Product line standard.

1.2.1 Line Printer

The LS11 is capable of interfacing a family of Centronics line printers to the Unibus, including Models 101, 101A*, 101D, 102A, and 303. These models are medium-speed serial matrix printers. The 101 model uses a 5 X 7 matrix; the 101A uses a 9 X 7 matrix. The 101 and 101A line printers have the following basic characteristics:

a. The average printing speed is 132 characters/second, including the return time of the printing head.

b. The line printing speeds are 60 lines/minute on full lines and up to 200 lines/minute on short lines.

c. The print size is 10 characters/inch horizontally and 6 lines/inch vertically.

The line printer contains a 132-character memory buffer, which is loaded character by character via the LS11 Controller. Once the 132-character memory is full, the Centronics printer automatically prints the 132 characters on a line and then performs an automatic carriage return. There is, however, a carriage return command, which is performed for lines containing less than 132 characters as specified by the programmer.

Each character is transferred to the line printer in a parallel 7-bit format. These 7-bit characters are in ASCII code (Appendix B). The Centronics line printer does not print lower case characters. Of the ASCII character set, the line printer uses nine commands. These commands and their functions are listed in Table 1-1. For more detailed printer information, refer to the applicable Centronics technical manual.

The front panel of the line printer unit contains four illuminated switches and one pushbutton switch, as follows:

a. Power On/Power Off Switch – alternate depression of this switch turns the printer on or off.

b. Select Switch – alternate depression of this switch places the printer in the on-line state (able to receive data) or the off-line state.

c. Top of Form – Depressing this switch causes the Vertical Format Reader to seek the Top-of-Form position as indicated by the paper tape.

d. Forms Override – Depressing this switch allows the printer to complete the form being printed, even though a Paper-Empty condition exists (Paper Out indicator is on).

NOTE

This indicator switch must be pressed and held during printing when a Paper-Empty condition exists.

e. Remote Line Feed – Depressing this switch initiates a single line feed.

The front panel also contains a Paper Out indicator, which, when lit, indicates that the paper supply rack is empty.

1.2.2 LS11 Controller

The LS11 Controller transfers a 7-bit (ASCII) character, in parallel, from the Unibus to the line printer. Software control of the LS11 Controller is implemented through the programmable Data Buffer Register (LSDB) and Status Control Register (LSCS). The characters are seven bits long and transfers are made using instructions to the low-order byte of the LSDB. The LS11 has four functional sections: Address Selector Logic, Interrupt Control Logic, Data Register Logic, and Printer Control Logic (Figure 1-2).

*Product line standard.

Table 1-1
Line Printer Commands and Functions

Octal ASCII Code	Character	Name	Function
007	BEL	Bell	Generates a 2-second audible tone from the speaker in the line printer unit.
012	LF	Line Feed	Performs a print cycle and a carriage return, and then advances the paper one line.
013	VT	Vertical Tab	Advances the line printer paper to the next hole position in Channel 2 of the line printer tape reader. Does not perform a carriage return or a print cycle.
014	FF	Form Feed	Performs a print cycle and a carriage return, then advances the paper to the next hole position in Channel 1 of the tape reader.
015	CR	Carriage Return	Causes all characters in the line printer character memory to be printed. There is no automatic line feed.
016	ELONG	Elongated Character	Doubles the size of horizontal printing axis, thus lowering the line capacity from 132 to 66 characters/line. This command code may be sent to the printer anywhere in a line, but, once sent, causes the entire line to be printed in the elongated format. The command must be given for each line to be elongated. If the character memory contains more than 66 characters when this command is in the line, then the 67th and all following characters are lost.
021	SEL	Select	Allows the program to place the printer on-line without having to depress the Select switch.
023	DSEL	Deselect	Allows the program to place the printer off-line without having to depress the Select switch.
177	DEL	Delete	Used to prime the Centronics line printer by destroying all characters in the character memory and performing a carriage return. There is no line feed, and printing does not occur.

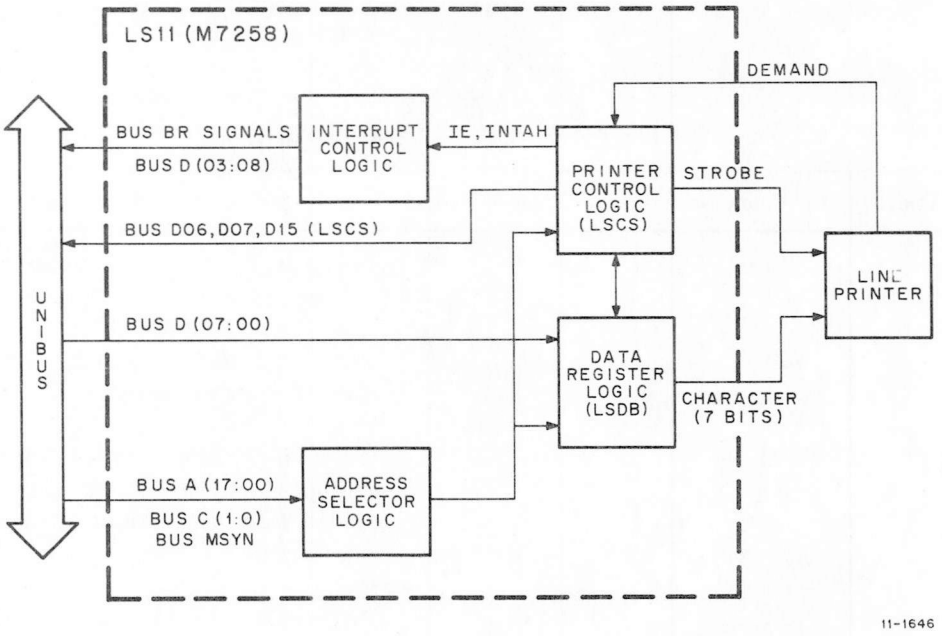


Figure 1-2 LS11 Functional Block Diagram

The address selector logic implements software control of the LS11 by recognizing when the LSDB or LSCS is addressed, as well as the Unibus operation (DATI or DATO for the LS11) to be performed. Characters are loaded from the Unibus by DATO or DATOB operations to the LSDB. The address selector also decodes read (DATI) and write (DATO or DATOB) instructions for the LSCS.

The interrupt control logic initiates processor interrupt action for the occurrence of an LS11 interrupt request condition. The interrupt request conditions are DONE set in the LSCS, which indicates that a character can be loaded into the character memory, or the occurrence of a line printer error condition (ERROR set in the LSCS). The interrupt control logic initiates a bus request for these conditions, when Interrupt Enable (IE) is set in the LSCS. The interrupt control then performs the interrupt sequence (Paragraph 4.3) on the Unibus to become bus master. When the LS11 is bus master, the interrupt control transfers the designated interrupt vector address to the processor. This vector address points the processor to a software service routine, which services the interrupt condition (refer to the *PDP-11 Peripherals and Interfacing Handbook*).

The printer control logic contains the LSCS, strobes each character from the LSDB into the line printer character memory, monitors line printer error conditions, and initiates interrupt requests to the interrupt control logic. In addition, for LP11 software compatibility, the printer control forces all FF or LF commands to the LSDB to transfer a CR command to the line printer before transferring the FF or LF character.

Line printer error conditions are: Hardware Alarm, Paper Out, Select, or Fault. A Paper Out error is indicated by the line printer indicator light. A Select error indicates that the line printer on-line switch is off. A Fault error indicates the occurrence of a Paper Out, Hardware Alarm, Select, or Light Detection error condition. A Light Detection error indicates that the line printer video lamp is inoperative. Any one of the above error conditions initiates an interrupt request from the interrupt control if Interrupt Enable is also set.

Table 1-2 lists the LS11 specifications. For line printer specifications, refer to the applicable Centronics technical manual.

Table 1-2
LS11 Specifications

Specification	Description
Options	LS11-A 115V, 60 Hz LS11-B 230V, 50 Hz
Power Requirement	+5V at 1.5A
Line Printer Characteristics (For models 101 and 101A only)	Print cycle speed: 132 characters/second Line printing speeds: 60 lines/minute (full lines) 200 lines/minute (short lines) Print size: 10 characters/inch horizontal 6 characters/inch vertical
Character Format	7-bit ASCII
Character Transfers	Parallel (seven bits of each character transferred in parallel)
Board Size	8-1/2 inch quad integrated circuit module

1.3 RELATED DOCUMENTS

Applicable documents pertaining to the LS11 Controller include the following:

a. *PDP-11 Peripherals and Interfacing Handbook* (Unibus Information)

b. Centronics (Models 101, 101A, 101D, 102A, or 303) printer technical manual

c. The respective PDP-11 system and processor manuals for the system containing the LS11

d. Any software documentation supplied with the PDP-11 system using the LS11

CHAPTER 2
INSTALLATION

2.1 INTRODUCTION

Installation information for the LS11 includes power and cabling requirements and the procedures necessary to make the LS11 operational, including selection of the LS11 M7258 module jumper configurations and installation testing. Installation information for the associated line printer is available in the applicable Centronics printer technical manual.

2.2 POWER REQUIREMENTS

Power for the LS11 Controller is wired to the DD11 System Unit by the power supply which is contained in the same PDP-11 mounting box as the unit it supplies.

2.3 CABLING REQUIREMENTS

Cabling requirements for the LS11 involve the Unibus connections and the line printer cable connection. Unibus connections are made according to the PDP-11 configuration selected, as described in the *PDP-11 Peripherals and Interfacing Handbook*. The line printer cable (D-IA-7009087-0-0) is connected to the M7258 Printer Interface Module as indicated in Figure 2-1.

2.4 JUMPER CONFIGURATIONS

The various selectable jumper terminal configurations of the LS11 and their functions are listed in Table 2-1.

Table 2-1
Selectable Jumpers

Jumpers	Function
V2 through V8	Select the vector address for the service routine for the LS11. Typically address 200 is used, which is configured by removing all V jumpers except V7.
A3 through A12	Select the device address to which the LS11 will respond. Typically an address from 777514 through 777517 is used. Address 777514 is selected when jumpers A7, A5, and A4 are in and the other A jumpers are removed.
J1 through J14 and W5	Configure the M7258 logic circuits for LS11 use. These jumpers are configured at the factory for use of the M7258 module with the LS11. This configuration is: IN– J2, J3, J5, J6, J9, J11, J14 OUT– J1, J4, J7, J8, J10, J12, J13, W5

Table 2-1 (Cont)
Selectable Jumpers

Jumpers	Function
N1	Controls sampling of the NPR line. In certain system configurations the NPR line can be sampled and interrupt requests prevented until all NPRs have been honored, thus improving NPR latency. Removal of the N1 jumper disables the NPR sampling circuit.

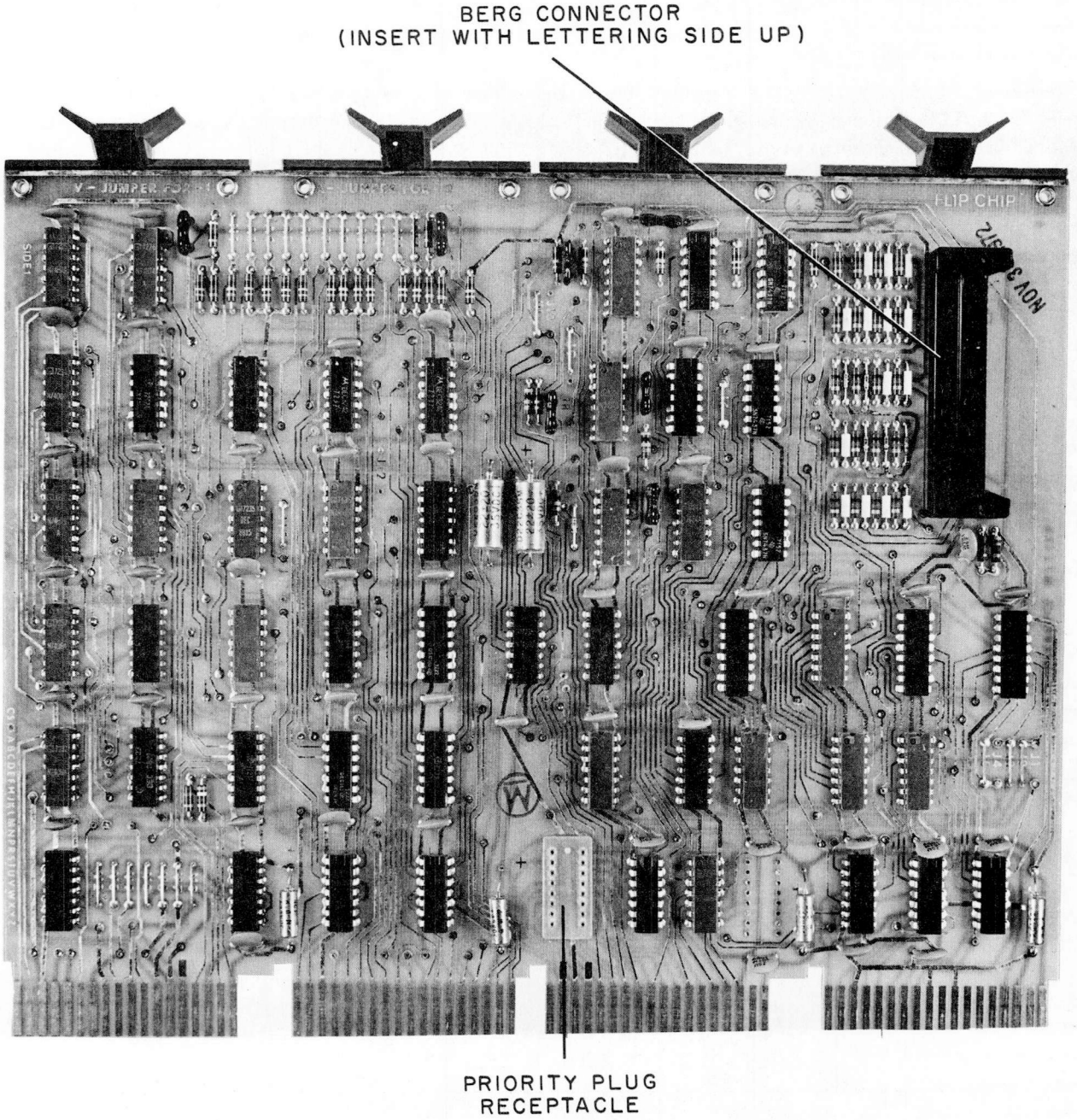


Figure 2-1 M7258 Printer Interface Module

2.5 INSTALLATION PROCEDURES

Before the LS11 is installed, the selectable jumpers should be in the desired configurations and the desired interrupt priority level plug (typically, BR4) should be plugged in. Also, the M7258 module should be checked for any sign of damage. The installation procedure for the LS11 is as follows:

1. Unpack and set up the Centronics printer, according to the instructions in the manual supplied with the printer.

2. Determine the proper slot for the LS11 module.

3. Remove the G727 Grant Continuity module from area D of the system unit slot.

4. Install the M7258 LS11 module in areas C through F of the appropriate slot.

5. Install the line printer cable into the connector on the M7258 in such a way that the printed lettering on the Berg side is visible (Figure 2-2).

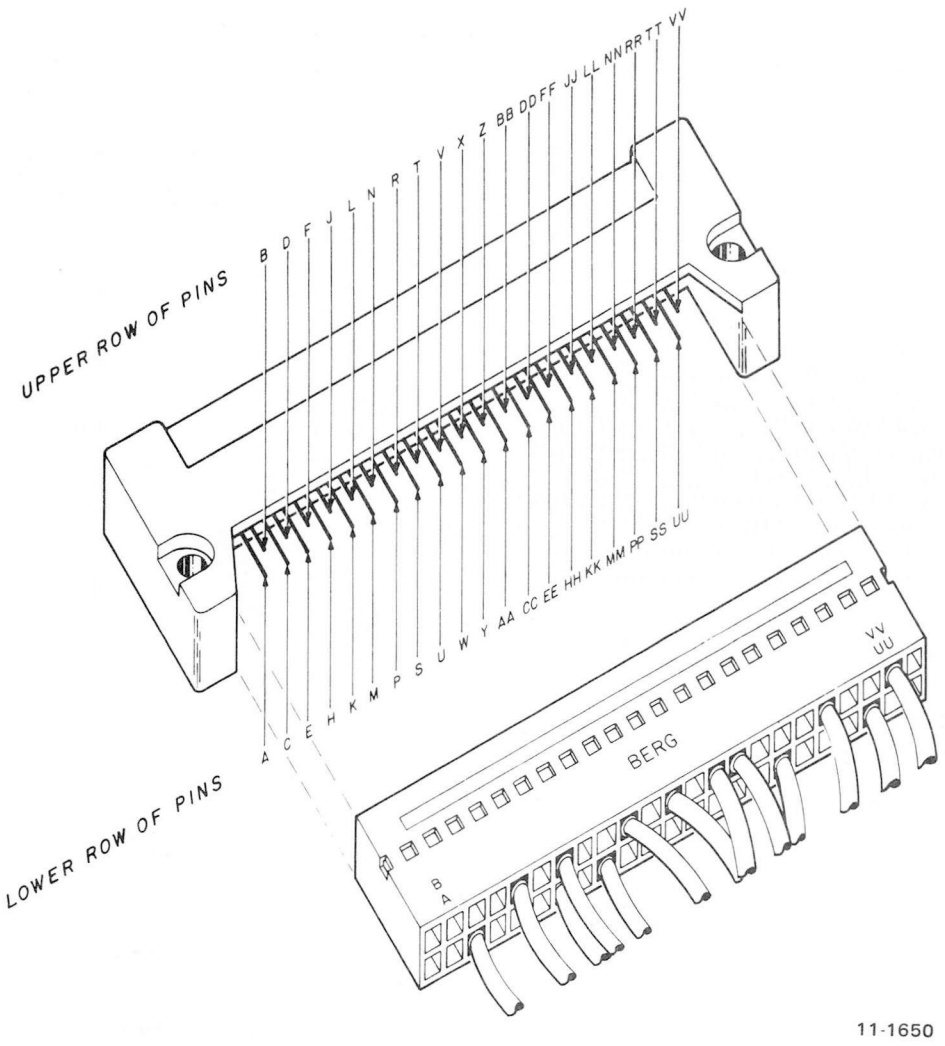


Figure 2-2 Berg Connector

Power is applied to the LS11 through the back panel of the PDP-11 system unit. When power is applied, the LS11 logic is initialized through BUS INIT on the Unibus.

2.6 INSTALLATION TESTING

When the LS11 and the Centronics printer have been installed and made operational, line printer checkout procedures should be performed (refer to Centronics printer technical manual). When printer checkout is complete, test the LS11 by running the MAINDEC-11–DZLSAA LS11 diagnostic program, which checks all LS11 logic. The diagnostic tape and program listing are supplied with the LS11.

CHAPTER 3
PROGRAMMING

3.1 INTRODUCTION

The software interface of the LS11 consists of two programmable device registers. These registers are assigned memory addresses, and can be read or loaded (with the exceptions noted) using any instruction that refers to their addresses.

ASCII-coded characters (Appendix B) are loaded into the line printer one character at a time. The characters are loaded into the printer memory from the LS11 programmable data buffer register (LSDB). When the printer memory is full (132 characters), the characters are automatically printed out. Special nonprinting characters serve as line printer commands and direct line printer functions as shown in Table 3-1. (These commands are defined more completely in Table 1-1.)

Table 3-1
Line Printer Commands

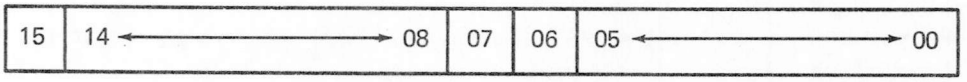
Mnemonic	Octal Code	Name
BELL	007	Bell
LF	012	Line Feed
VT	013	Vertical Tab
FF	014	Form Feed
CR	015	Carriage Return
ELONG	016	Elongated Character
SEL	021	Select
DSEL	023	Deselect
DEL	177	Delete

3.2 PROGRAMMABLE DEVICE REGISTERS

In the two programmable device registers, unused and Read Only bits are always read as zeros. Loading unused and Read Only bits has no effect on the bit. INIT refers to the initialization signal generated by the processor when powering up and powering down or for a RESET instruction, as well as by the depression of START on the processor console.

3.2.1 Control and Status Register (LSCS)

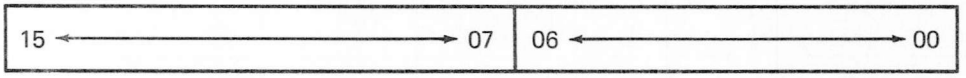
Address: 777514



Bit	Name	Definition
15	ERROR	ERROR asserted indicates the Inclusive OR of one of the following line printer error conditions: a. Paper Empty b. Hardware Alarm c. Light Detection d. Select ERROR is Read Only, and is reset only when the error condition is removed. If Interrupt Enable is also set, the LS11 starts an interrupt sequence.
14–08		Unused
07	DONE	DONE is asserted when the line printer is ready to accept another character. DONE is set by INIT and cleared by loading the LSDB. If Interrupt Enable is also set, the LS11 starts an interrupt sequence.
06	IE	Interrupt Enable is set or cleared by the program and cleared by INIT. Either DONE or ERROR set when IE is set initiates an interrupt sequence.
05–00		Unused

3.2.2 Data Buffer Register (LSDB)

Address: 777516



Bit	Name	Definition
15–07		Unused
06–00	DATA	The Data bits are the 7-bit characters transferred to the line printer. The characters are coded in ASCII and are Write Only.

3.3 ADDRESSES

Addresses 777510 and 777512 are unused for the LS11 and will not respond when addressed (NO SSYN). The LS11 Controller will respond to 777514 (LSCS) and 777516 (LSDB).

The Unibus address contains 18 bits [A(17:00)], offering the capability of addressing 256K memory locations, each of which is an 8-bit byte. The basic PDP-11 processors provide program control for only 16 bits of address information, which address a maximum of 64K bytes or 32K words. The address word length and bus width in these processors are 16 bits (2 bytes). A word operation accesses two locations at once. The Unibus word address contains the even-numbered location only, and the next higher odd location is selected also to provide a 16-bit word. A byte operation accesses an odd or even location to select an 8-bit byte.

When a PDP-11 processor with a maximum limit of 64K memory locations is used, bits A17 and A16 are forced to 1s if bits A(15:13) are all 1s when the processor is master. With bits A(17:13) all 1s, the last 8K locations are relocated to become the highest locations accessible by the bus. All device addresses and internal processor locations are assigned in these 8K locations. The assigned addresses for the LS11 Controller registers are in these locations.

3.4 INTERRUPTS

A program interrupt sequence is initiated when ERROR or DONE is set and Interrupt Enable (IE) has been set in the LSCS. When the LS11 is granted control of the Unibus, it points the processor to a software interrupt routine through the LS11 vector address (typically 200) at the normal LS11 priority level (Level 4). The LP11 line printer also utilizes this vector address and priority level.

3.5 LS11 vs LP11

Because the LS11 and the LP11 occupy the same register address locations, vector address location, and priority level, it is advantageous that they both utilize the same software. The significant differences between the LS11 and the LP11 are in the respective character commands. The software-related differences are listed in Table 3-2.

Both the LP11 and the LS11 will print when their buffers are full, but the buffer sizes are 20 and 132 characters, respectively.

Common drivers for the LS11 and the LP11 can be written, provided the following differences are noted:

a. No DEL (177_8) or ELONG (016_8) codes can be issued.

b. The VT (013_8) feature cannot be used.

c. All letters must be upper case.

d. The Centronics tape for a FF must slew the proper number of lines.

e. An 80-character line must be used if a 132-character LP11 is not available.

f. No SEL (021_8) or DSEL (023_8) codes can be issued.

Table 3-2
LS11 and LP11 Commands

Command	LS11	LP11
007_8	BELL (A 2-second audible tone)	Prints a space
012_8	LF – Line Feed 1. Print cycle 2. Carriage return 3. Advances paper one line	PF – Paper Feed 1. Print cycle 2. Carriage return 3. Advances paper one line
013_8	VT – Vertical Tab 1. Advances paper to the next hole position in Channel 5	VT – Vertical Tab 1. Prints a space
014_8	FF – Form Feed 1. Print cycle 2. Carriage return 3. Advances paper to the next hole position in Channel 7	FF – Form Feed 1. Print cycle 2. Carriage return 3. Advances paper to the third line of the next form
015_8	CR – Carriage Return 1. Print cycle 2. Carriage return 3. No line feed	CR – Carriage Return 1. Print cycle 2. Carriage return 3. No line feed
016_8	ELONG – Elongated Character 1. Doubles the horizontal printing axis	ELONG – Elongated Character 1. Prints a space
021_8	SEL – Select 1. Allows the software to put the printer on-line	SEL – Select 1. Prints a space
023_8	DSEL – Deselect 1. Allows the software to put the printer off-line	DSEL – Deselect 1. Prints a space
177_8	DEL – Delete 1. Destroys all characters in the memory buffer 2. Carriage return 3. No line feed 4. No printing	DEL – Delete 1. Prints a space

3.6 PROGRAM EXAMPLES

The following examples represent typical programs used to control the line printer (LS11/LP11) by means of an interrupt service routine.

The first routine requires 18 words. This routine may be speeded up by saving and restoring R1, R2, and R3, and loading these registers with the LPCS, LPDA, and BUFFEND values.

a. Interrupt Service Routine (Example 1)

```
                177514                          LPCS=177514                     ;CONTROL AND STATUS
                                                                                ;REGISTER
                177516                          LPDB=177516                     ;DATA BUFFER REGISTER
                000007                          SP=%7

                000200                          .=200                           ;ORIGIN FOR LPT VECTOR
000200          002000                          .WORD   LPSERV                  ;VECTOR TO SERVICE
                                                                                ;ROUTINE
000202          000200                          .WORD   200                     ;SERVICE AT PRIORITY
                                                                                ;LEVEL 4
                001000                          .=1000
001000          001000                          .
001002          052767  000100  176504  MAIN:   BIS     #100,   LPCS            ;ENABLE INTERRUPT
001010          001010                          .
001012          001012                          .
                002000                          .=2000
002000          005767  175510          LPSERV: TST     LPCS                    ;CHECK FOR ERROR
002004          100417                          BMI     ERROR
002006          010047                          MOV     %0,     -(SP)           ;SAVE R0
002010          016700  000030                  MOV     BUFADR, %0              ;GET BUFFER POINTER
002014          112067  175476          LOAD:   MOVB    (%0) +, LPDB            ;LOAD PRINTER BUFFER
002020          020067  000020                  CMP     %0,     BUFEND          ;END OF DATA?
002024          101007                          BHI     PRCOMP                  ;YES, GO TO PRINT
                                                                                ;COMPLETE
002026          105767  175462                  TSTB    LPCS                    ;NO, CHECK READY
002032          100770                          BMI     LOAD                    ;NOT FULL, GET ANOTHER
                                                                                ;CHARACTER
002034          010067  000004          EXIT:   MOV     %0,     BUFADR          ;SAVE BUFFER POINTER
002040          012700                          MOV     (SP) +, %0              ;RESTORE R0
```

(continued on next page)

```
002042  000002                          RTI             ;BACK TO MAIN PROGRAM

                                BUFADR:                 ;BUFFER DATA POINTER
                                BUFEND:                 ;BUFFER END ADDRESS
                                ERROR:                  ;START OF ERROR
                                                        ;ROUTINE
                                PRCOMP:                 ;START OF ROUTINE FOR
                                                        ;PRINTER COMPLETE
        000001                          .END

                                BUFADR  002044
                                BUFEND  002044
                                ERROR   002044
                                EXIT    002034
                                LOAD    002014
                                LPCS    177514
                                LPDB    177516
                                LPSERV  002000
                                MAIN    001002
                                PRCOMP  002044
                                SP      000007R

ERRORS DETECTED:  0
RUN-TIME:  0 SECONDS
4K CORE USED
```

b. **Interrupt Service Subroutine (Example 2)**

```
                ;REGISTERS
000000  R0      =       %0
000001  R1      =       %1
000002  R2      =       %2
000003  R3      =       %3
000004  R4      =       %4
000005  R5      =       %5
000006  SP      =       %6
000007  PC      =       %7
                ;INTERRUPT DRIVEN LINE-PRINTER SUBROUTINE
                ;
                ;CALL:  MOV     #PARAM,R0       ;ADDRESS OF PARAMETER BLOCK
                ;       JSR     PC,LPTIO        ;CALL LPT DRIVER
                ;       .WORD   INIERH          ;INITIALIZATION ERROR ADDRESS
                ;       . . .                   ;NORMAL RETURN – I/O IN PROGRESS
```

(continuted on next page)

```
                        ;           ...
                        ;
                        ;THE PARAMETERS ARE:
                        ;PARAM:  .WORD   LPCOUNT     ;POSITIVE BYTE COUNT
                        ;        .WORD   LPBUF       ;DATA BUFFER ADDRESS
                        ;        .WORD   LPRET       ;SUBROUTINE ADDRESSES:
                        ;                            ;   LPRET FOR ON-LINE ERRORS
                        ;                            ;   LPRET+2 FOR NORMAL I/O COMPL
                        ;
                        ;LINE PRINTER DEVICE REGISTERS:
                        ;
          177514        LPCS    =       177514      ;CONTROL AND STATUS
          177516        LPDB    =       177516      ;DATA BUFFER
                        ;
                        ;INITIALIZE OPERATION
                        ;
000000    005767        LPTIO:  TST     LPCS        ;LINE PRINTER OK?
          177510
000004    100001                BPL     .+4         ;YES
000006    013607                MOV     @(SP)+,PC   ;NO – POP INITIALIZATION ERROR A
000010    062716                ADD     #2,(SP)     ;SKIP OVER ERROR ADDRESS
          000002
000014    010067                MOV     R0,LPTPAR   ;SAVE PARAMETER ADDRESS
          000010
000020    012767                MOV     #100,LPCS   ;ENABLE INTERRUPT, AND THEN INT
          000100
          177466
000026    000207                RTS     PC          ;RETURN
000030    000000        LPTPAR: .WORD   0           ;ADDRESS OF PARAMETERS
                        ;
                        ;SERVICE INTERRUPTS
                        ;
000032    010046        LPTINT: MOV     R0,-(SP)    ;SAVE R0, R1, R2 ON STACK
000034    010146                MOV     R1,-(SP)
000036    010246                MOV     R2,-(SP)
000040    016700                MOV     LPTPAR,R0   ;POINTS TO PARAMETER BLOCK
          177764
000044    012701                MOV     #LPCS,R1    ;POINTS TO STATUS REGISTER
          177514
000050    012702                MOV     #LPDB,R2    ;POINTS TO DATA REGISTER
          177516
000054    005711                TST     (R1)        ;ANY ERRORS?
000056    100003                BPL     .+10        ;NO
000060    004770                JSR     PC,@4(R0)   ;YES – GO TO ERROR SUBROUTINE
          000004
000064    000411                BR      LPTIN3      ;CLEAN UP STACK AND EXIT
000066    005720                TST     (R0)+       ;MAKE R0 POINT TO BUFFER ADDRESS
000070    005740        LPTIN1: TST     -(R0)       ;TEST BYTE COUNT
000072    001412                BEQ     LPTIN2      ;YES – DONE
```

(continued on next page)

```
000074  005320          DEC     (R0)+           ;DECREMENT COUNT
000076  117012          MOVB    @(R0),(R2)      ;MOVE CHARACTER TO LPDB
        000000
000102  005210          INC     (R0)            ;UPDATE BUFFER POINTER
000104  105711          TSTB    (R1)            ;IS PRINTER READY?
000106  100770          BMI     LPTIN1          ;YES – MOVE IN ANOTHER CHARACTER
000110  012602  LPTIN3:  MOV     (SP)+,R2        ;RESTORE R2, R1, R0
000112  012601          MOV     (SP)+,R1
000114  012600          MOV     (SP)+,R0
000116  000002          RTI                     ;RETURN
000120  005011  LPTIN2:  CLR     (R1)            ;DISABLE THE INTERRUPT
000122  016001          MOV     4(R0),R1        ;TRANSFER COMPLETE – SET UP CALL
        000004
000126  062701          ADD     #2,R1           ;TO COMPLETION ROUTINE
        000002
000132  004711          JSR     PC,(R1)         ;NOW CALL IT
000134  000765          BR      LPTIN3          ;CLEAN UP STACK AND EXIT
        000200          .=200                   ;ORIGIN FOR LPT VECTOR
000200  000032          .WORD   LPTINT          ;INTERRUPT HANDLER
000202  000200          .WORD   200             ;PRIORITY 4
        000001          .END

LPCS    = 177514        LPDB    = 177516        LPTINT  000032  LPTIN1  000070
LPTIN2  000120          LPTIN3  000110          LPTIO   000000  LPTPAR  000030
PC      =%000007        R0      =%000000        R1      =%000001  R2    =%000002
R3      =%000003        R4      =%000004        R5      =%000005  SP    =%000006
        = 000204
```

CHAPTER 4
DETAILED DESCRIPTION

4.1 INTRODUCTION

The following paragraphs provide a logic level description of the functional units into which the LS11 M7258 module is divided (Figure 1-2): Address Selector, Interrupt Control, Data Register, and Printer Control. Some of the LS11 logic is implemented with MSI integrated circuits (ICs). Appendix A contains logic diagrams with pin designations of each MSI IC used. The LS11 logic can be found on engineering drawing D-CS-M7258-0-1 (Printer Interface), Sheets 1 through 4. These sheets are, respectively, the cover sheet (sheet P-1), the Data Register (sheet P-2), the Printer Control (sheet P-3), and the Address Selection and Interrupt Control (sheet P-4).

4.2 ADDRESS SELECTION

The address selection logic (sheet P-4) decodes the address information from the bus and provides three gating signals (only two are used) and four select line signals (two are used) to control the LS11 Controller registers. Jumpers are arranged so that the module responds only to the standard device register addresses 777514–777517 (jumpers in A4, A5, A7, J14). Although these addresses have been selected by Digital Equipment Corporation as the standard address assignments for the LS11 Controller, the customer may change the jumpers to any address desired. However, any MAINDEC program that references the LS11 Controller standard address assignments must be modified to reflect the new assignments.

The first five octal digits of the address (77751x) indicate that the LS11 has been selected as the device to be used. The final octal digit, consisting of A02, A01, and A00, determines which register has been selected and whether a word or byte operation is to be performed. The two mode control lines, C00 and C01, determine whether the selected register is to perform an input or output function. The three jumpers, J12, J13, and J14, determine the responses to the last octal digit of the address as follows:

J12 – A response only from 0 and 2; no response (no SSYN) from 4 and 6.

J14 – A response only from 4 and 6; no response (no SSYN) from 0 and 2 (standard).

J13 – A response from 0, 2, 4, and 6.

4.2.1 Inputs

A simplified block diagram of the address selection logic is shown in Figure 4-1. Note that IN and OUT are always used with respect to the master (controlling) device. Thus, when the line printer controller is used, an OUT transfer is a transfer of data out of the master (the processor) and into the device. Likewise, an IN transfer is the operation of the controller furnishing data to the processor.

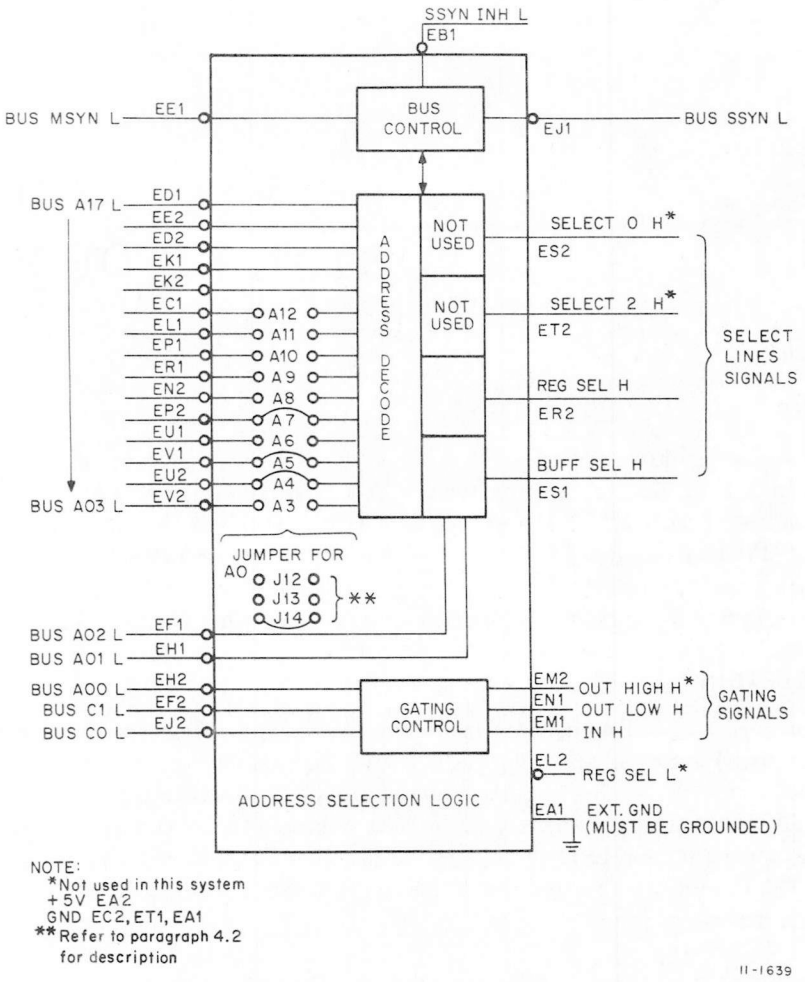


Figure 4-1 Address Selection Logic, Simplified Diagram

The address selection logic input signals consist of 18 address lines, A(17:00), two bus control lines C(01:00), and a master synchronization, MSYN, line. The address selection logic decodes the incoming address as described below. This address format is shown in Figure 4-2. Note that all input gates are standard bus receivers.

a. Line A00 is used for byte control.

b. Lines A01 and A02 are decoded to select one of the two control registers (status or data buffer).

c. Decoding of lines A(12:03) is determined by jumpers. When a given line contains a jumper, the address logic searches for a 0 on that line. If there is no jumper, the logic searches for a 1.

NOTE

Connection of address jumpers on the M7258 quad module is identical to the method used on models which employed an M105 Address Selector Module.

d. Address lines A(17:13) must be all 1s. This specifies an address within the top 8K byte address bounds for device registers.

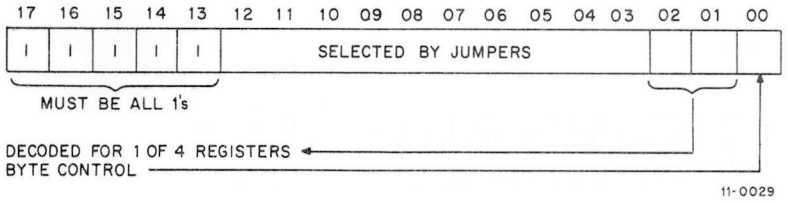

17 16 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
1 1 1 1 1
SELECTED BY JUMPERS
MUST BE ALL 1's
DECODED FOR 1 OF 4 REGISTERS
BYTE CONTROL
11-0029

Figure 4-2 Controller Select Address Format

4.2.2 Outputs

The address selection logic output signals permit selection of two 16-bit registers and provide three signals that are used for gating information into and out of the master device. All of the output signals are listed in Table 4-1. Note, however, that only two gating signals are listed (IN and OUT). Actually, there are two OUT signals, OUT LOW and OUT HIGH, but OUT HIGH is not used by the LS11 Controller. The logic diagram (sheet P-4) shows two additional select line signals, SELECT 0 and SELECT 2. Neither of these signals is used by the controller.

Tables 4-1 and 4-2 indicate the input signals that select the control output line states.

Table 4-1
Select Lines

Input Lines A (02:01)	Select Lines True (+3V)
00, 10	0 not used
01, 11	2 not used
00, 10	Reg Sel
01, 11	Buf Sel

NOTES: 1. Lines A(17:13) must be all 1s (0V on Unibus).
2. Lines A(12:03) are selected by jumpers.
3. J12, J13, and J14 determine if 00, 01 or 10, 11 pairs are used.

Table 4-2
Gating Control Signals

Mode Control C(01:00)	Byte Control A00	Gating Control Signals True (+3V)	Bus Sequence
00	0	IN	DATI
00	1	IN	DATI
01	0	IN	DATIP
01	1	IN	DATIP
10	0	OUT LOW OUT HIGH	DATO
10	1	OUT LOW OUT HIGH	DATO
11	0	OUT LOW	DATOB
11	1	OUT HIGH	DATOB

NOTES: 1. Gating control signals may become true although select lines are not.
2. OUT HIGH not used in LS11 Controller.

4.2.3 Slave Sync (SSYN)

When SSYN INH is grounded, it inhibits the acknowledgement signal (SSYN) normally generated by the address selection logic.

4.3 INTERRUPT CONTROL

The interrupt control logic (sheet P-4) permits the LS11 Controller to gain control of the bus (become bus master) and perform an interrupt operation. The jumpers on this logic are arranged so that the logic has a normal vector address of 200 (jumper in bit position 07). Although this is the recommended vector address, the user may change the jumpers to correspond to any address desired, but MAINDEC programs and other software referencing the standard vector address assignment of 200 **must** be changed to reflect the new assignments.

NOTE

Connection of interrupt control jumpers on the M7258 quad module is the *reverse* of the method used on M782 and M7820 Interrupt Control Modules, and the same as the M7821 module. On the M7258 module, a jumper represents a 1; no jumper represents a 0.

The interrupt control logic consists of a dual-input request and grant acknowledge circuit for establishing bus control. The interrupt occurs at vector address 200. The B input portion of the logic is disabled because neither an INT B or INT ENB B can be generated by the LS11 Controller (these two input lines are grounded as shown on sheet P-3).

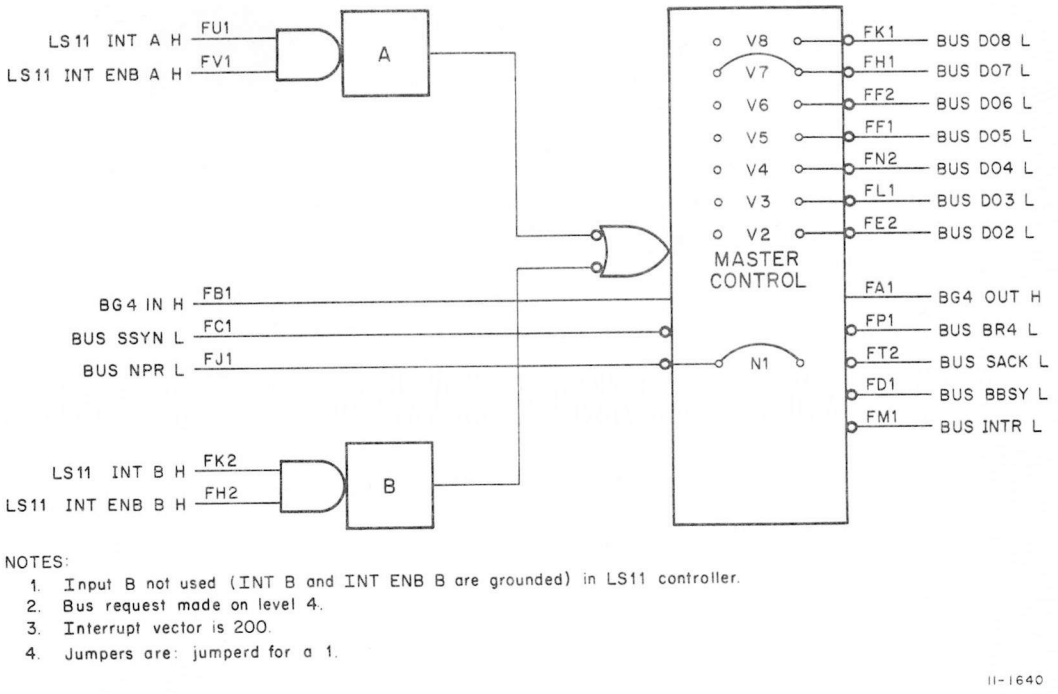
Before the interrupt control logic can generate an interrupt request, two input signals must be high: INT A and INT ENB A. The logic that generates these two signals is shown on sheet P-3. When a 1 is loaded into bit 06 of the status register, it sets the INT ENB flip-flop to produce INT ENB A H. The data input to this flip-flop is the 1 from BUS D06 and the clock input is the load signal (REG SEL H and OUT LOW H).

The second signal that must be present to generate an interrupt is INT A H. The INT A H signal is produced by an OR gate and an inverter that is qualified when either a DONE or an ERROR condition exists. The DONE and ERROR conditions are described in Paragraph 4.5.

The master control section of the interrupt logic (Figure 4-3) is used to gain control of the bus. When both the INT A and INT ENB A requesting inputs are asserted, a bus request is made on the BR level corresponding to the level of the priority plug. The standard level for the LS11 Controller is BR4, but this may be changed by the priority plug, if desired. When the priority arbitration logic in the processor recognizes the request and issues a bus grant signal, the master control circuit acknowledges with a SACK signal. When the controller has fulfilled all requirements to become bus master (BBSY false, SSYN false, BG false), the master control section asserts BBSY.

Once the controller has gained bus control by means of a BR request, an interrupt is generated. The interrupt vector address is selected by jumpers on the logic shown on Figure 4-3. Because the vector is a 2-word (4-byte) block, it is not necessary to assert the state of bits 00 and 01. The seven selectable lines determine the vector addresses.

The BG IN signal is allowed to pass through the logic to BUS BG OUT when the controller is not issuing a request. To request bus use, the AND condition of INT A and INT ENB A must be satisfied. These levels must be true until the interrupt service routine clears INT or INT ENB. Once bus control has been attained, it is released when the processor responds with BUS SSYN after it has strobed in the interrupt vector. After releasing bus control, the logic inhibits further bus requests even if INT A and INT ENB A remain asserted. In order to make another request, INT A or INT ENB A must be dropped and then reasserted to cause the logic to reassert the request line. This prevents multiple interrupts when the master control is used to generate interrupts.



NOTES:
1. Input B not used (INT B and INT ENB B are grounded) in LS11 controller.
2. Bus request made on level 4.
3. Interrupt vector is 200.
4. Jumpers are: jumperd for a 1.

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Figure 4-3 Interrupt Control Logic, Simplified Block Diagram

Note that the interrupt control logic used in the LS11 Controller is not capable of issuing NPR requests. In order to improve NPR latency, the NPR line is sampled and prevents an interrupt request until all NPRs have been honored. The sampling of the NPR line is controlled by a jumper (N1) on the controller module.

CAUTION

Only certain PDP-11 processors can work with the special circuits described above. The jumper (N1) on the module, when cut, prevents the special circuit from working.

4.4 DATA REGISTER LOGIC

The data register logic (sheet P-2) transfers each character from the Unibus to the line printer, forces all lower case designated characters to upper case, detects a DEL (Delete), LF (Line Feed), or FF (Form Feed) line printer command (nonprinting character), and causes FF and LF commands to perform a CR command before receiving the LF or FF. A 7-bit character is received by the data register logic from BUS D00 L through BUS D06 L (a low asserts a 1 on the Bus D lines). This character is clocked into two 74175 D-type flip-flop ICs, which form the 7-bit Data Register or LSDB, by BUFFER SEL H and OUT LOW H, which are asserted by the address selector logic. OUT LOW H indicates a DATO or DATOB bus operation, and BUFFER SEL H indicates that the LS11 is selected. OUT LOW H and BUFFER SEL H also generate LD BUF H. The Data Register is loaded by addressing the LSDB and initiating a DATO transfer.

The feature of forcing all lower case characters (character codes 140_8 to 176_8) to upper case (character codes 100_8 to 136_8) is jumper selectable (J2 enables it) at the BUS D05 L input to the 74175 IC. The jumpered bit 05 of the character code is 1 (BUS D05 L asserted) for lower case characters and 0 (BUS D05 L unasserted) for upper case characters (Appendix B). Therefore, to convert lower case characters to their upper case equivalents, the bit 05 input to the LSDB (74175 IC) is forced to a 0 (L) for all lower case characters loaded from the Unibus. This is implemented when BUS D06 L is asserted (1), indicating that the character is to be converted and that the character

is not a DELETE command (177_8). These conditions enable the 7400 gate, which, through the 7408 gate, forces bit 05 to 0 at the 74175 IC input. For example, bit 05 for lower case "a" (141) is converted from 1 to 0, which changes to the code upper case "A" (101). If the character designates a DELETE command (DELETE L asserted), the 7400 is inhibited. For all other characters this gating logic is inhibited by BUS D06 L unasserted. In this case, the bit 05, 74175 IC input is determined by the BD05 H input to the 7408 gate. With the character in the Data Register, the 74175 IC outputs are, in turn, driven to the line printer by 7437 driver gates. The 74175 IC outputs are also checked to indicate an LF or FF command. If the octal code 012_8 or 014_8 is contained in the LSDB, then LF/FF L is asserted when GATE H is generated by the printer control logic.

HOLD (1) L from the printer control logic indicates that an LF or FF command is in the Data Register. When HOLD is set, the printer control cycles once to enable a CR at the line printer outputs. HOLD (1) L asserted does the conversion by forcing bits 00–02 (P DATA 1 H through P DATA 3 H) of the LF or FF character code to an octal 5 (101). This converts a 012_8 (LF) to 015_8 (CR) and a 014_8 (FF) to a 015_8 (CR). Once the CR is transferred to the line printer, the LF or FF in the LSDB is, in turn, transferred to the line printer.

The Data Register logic also contains the interrupt Priority Plug. The LS11 is, typically, configured with a BR4 interrupt level Priority Plug.

4.5 PRINTER CONTROL LOGIC

The printer control logic (sheet P-3) monitors line printer control lines, initiates interrupt requests in the interrupt control logic, contains the LSCS bits, and provides a STROBE signal to the line printer, which loads each character from the LSDB into the line printer buffer. In addition, the printer control logic controls holding of the Data Register (LSDB) and implements a CR command before the LF or FF command at the LSDB's output to the line printer.

For normal transfers of all characters to the line printer, except LF and FF, refer to the timing diagram of Figure 4-4. LD BUF H, asserted by the data register logic, indicates when the address selector logic loads the LSDB. The trailing edge fires a 74123 one-shot (A) generating a 500 ns pulse whose trailing edge fires another 74123 one-shot (STROBE), which generates another 500 ns pulse. The STROBE one-shot output drives STROBE L (DSTB) to the line printer, which strobes the LS11 Data Register Character into the line printer buffer. LD BUF H also clears the DONE flip-flop on its leading edge and on its trailing edge fires another 74123 one-shot, producing GATE H. (DONE is initially set by BUS INIT L.) GATE H inputs the data register logic to generate LF/FF L, if an LF or FF character is contained in the LSDB. With LF/FF L unasserted, the HOLD flip-flop remains clear and P DEMAND H, asserted by the line printer, sets DONE. P DEMAND H ($\overline{\text{ACKNLG}}$) asserted indicates that the line printer has loaded the character. DONE set, in turn, generates an interrupt request (INT A H), if IE is set in LSCS (INT ENB A H asserted). The processor can then service the DONE interrupt by sending another character to the LSDB.

If, when GATE H is asserted, LF/FF L is generated by the data register logic, indicating an LF or FF in the LSDB, the HOLD flip-flop is set (Figure 4-5). HOLD set inhibits the setting of DONE and changes the FF or LF character code to a CR character code at the line printer output lines in the data register logic (Paragraph 4.4). Therefore, when the converted CR is loaded into the line printer by STROBE L, P DEMAND H does not set DONE, but clears HOLD. HOLD going clear, in turn, fires a 200 ns one-shot. The trailing edge of this 200 ns pulse, like LD BUF H, fires the A one-shot. The sequence then proceeds the same as a normal character transfer. The STROBE one-shot is fired by A's trailing edge to generate STROBE L, which loads the LF or FF character still in the LSDB into the line printer buffer. With HOLD now clear, P DEMAND H sets DONE.

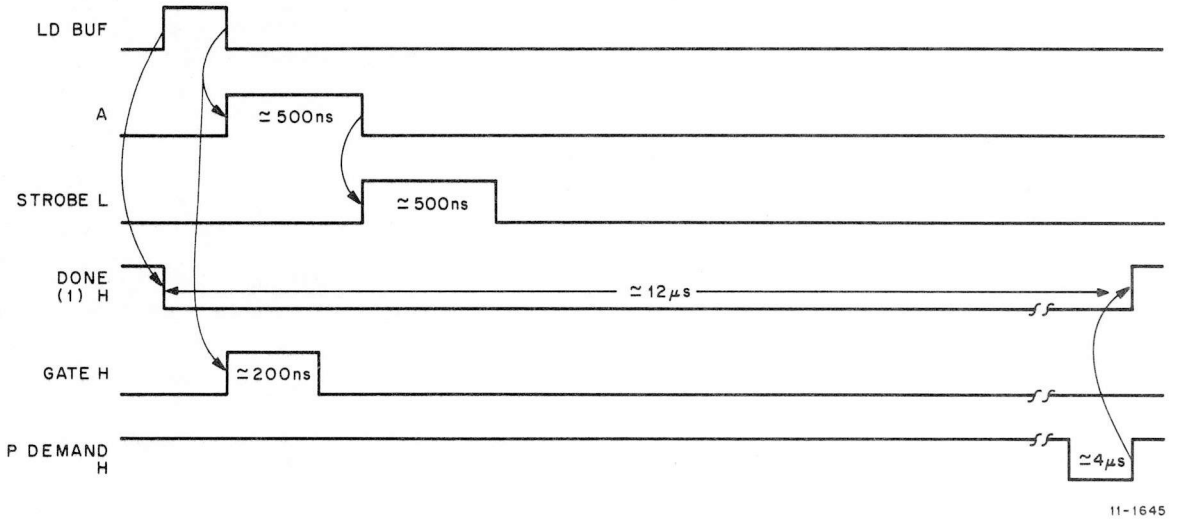


Figure 4-4 LS11 Character Transfer Timing Diagram

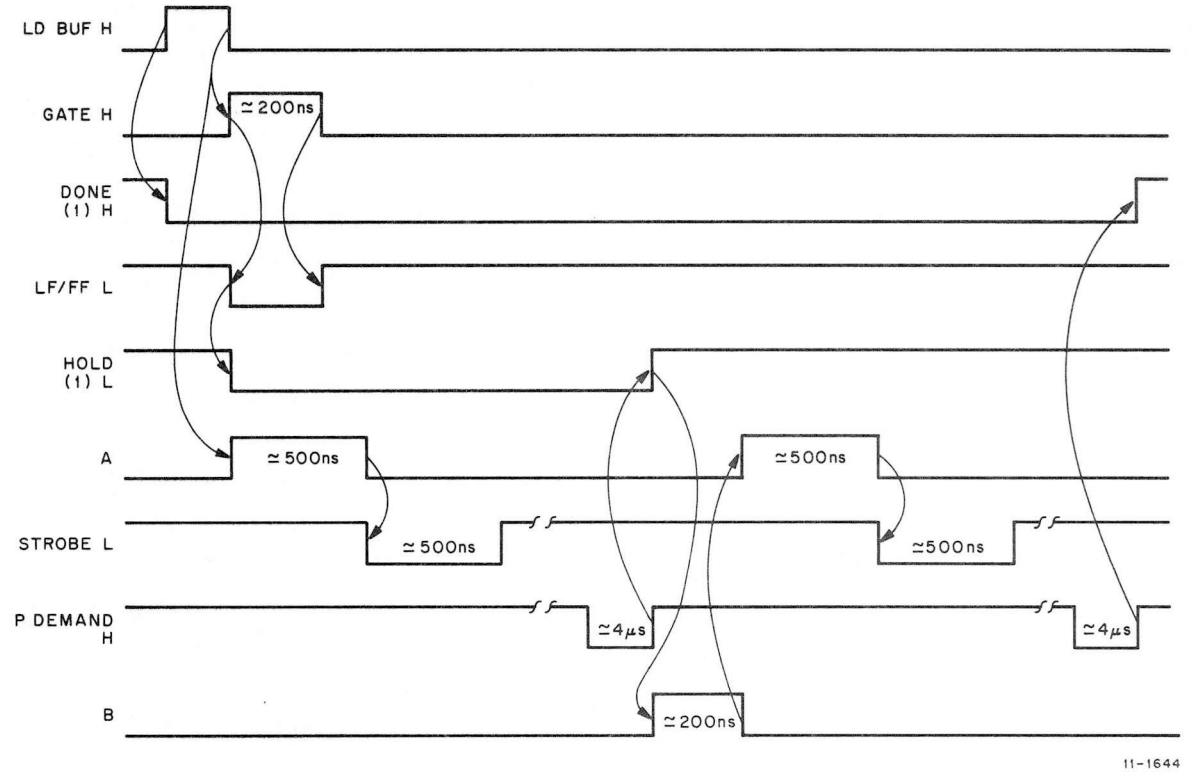


Figure 4-5 LF and FF Timing Diagram

The printer control logic also generates INT A H when ERROR H is generated (bit 15 of the LSCS). If P FAULT L, P HDWR H, P PAPER H, or P SELECT L is asserted from the line printer, ERROR H is generated for at least 400 ms by a 74123 one-shot. ERROR H, in turn, generates INT A H and inhibits DONE from being read by the program. Therefore, ERROR H or DONE (1) H generates INT A H, which generates an interrupt request from the interrupt control logic if IE of the LSCS is set.

IE (bit 06 of the LSCS) is loaded from the Unibus when the LSCS register is addressed for a DATO bus operation. The LSCS is available to the Unibus by addressing the LSCS for a DATI operation. IN H and STATUS SEL H asserted drive bits 06 (IE), 07 (DONE), and 15 (ERROR) onto the respective Unibus D lines.

The 74174 IC logic used to generate BUF CLR, REM EOT, REM FF, LINE TERM, and MODE is not used by the LS11 in interfacing with a Centronics printer. This logic is disabled with jumper J10 removed and J11 inserted.

CHAPTER 5
MAINTENANCE

5.1 INTRODUCTION

Maintenance of the LS11 consists of inspection and diagnostic procedures. Line printer maintenance information may be found in the *Centronics Printer Technical Manual* for the particular printer. The engineering drawings in the *Engineering Drawings Manual* are also used to locate points in the logic and on the M7258 module.

5.2 INSPECTION

Inspection of the LS11 is by means of a visual check to ensure that the configuration is correct and that the equipment has not been damaged. The inspection procedure is as follows:

1. Remove and check the M7258 for broken connections or damaged components. Look for discoloration of any surfaces or loose solder joints. Check that the address and vector jumpers are properly inserted, and that the BR4 priority plug (Part No. 5408776) is installed.

2. Check the line printer cable for damage and proper connection to the M7258 (the side of the Berg connector with lettering on it must be visible).

3. Check that the M7258 is plugged into the correct slots and system unit firmly, according to the applicable PDP-11 system scheme.

5.3 DIAGNOSTICS

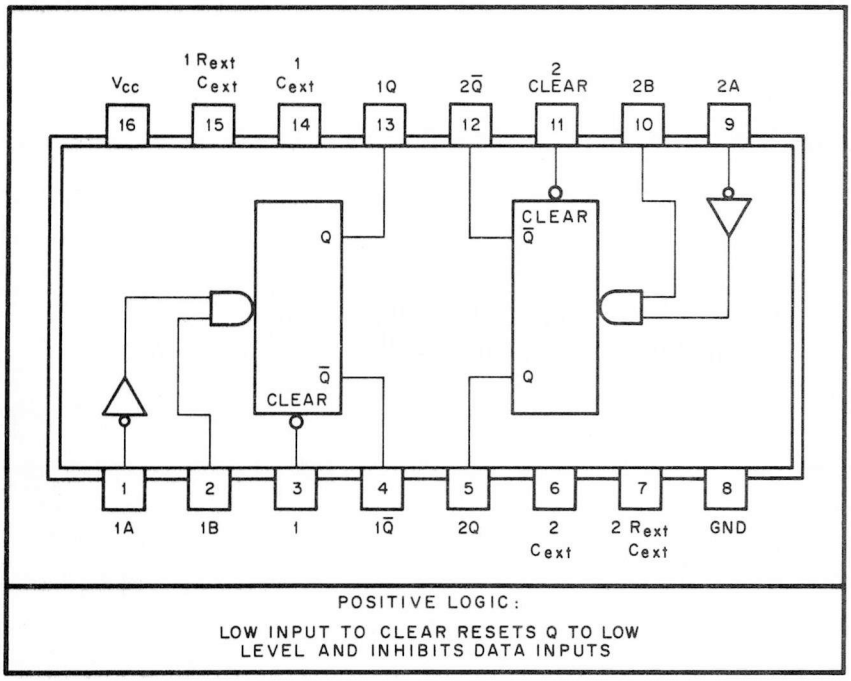
The LS11 logic is completely checked by running the MAINDEC-11-DZLSAA diagnostic program (LS11 Centronics Printer Test). This program, including a program listing, is supplied with each LS11 shipped. The program listing contains a program description and explanation, along with instructions for running the diagnostic. Running the LS11 diagnostic program provides a trouble-shooting feature for locating LS11 hardware malfunctions.

APPENDIX A
LS11 INTEGRATED CIRCUITS

The LS11 uses the following MSI integrated circuits (IC) in its logic. Functional logic diagrams and pin designation diagrams are provided.

TRUTH TABLE

INPUTS		OUTPUTS	
A	B	Q	$\overline{Q}$
H	X	L	H
X	L	L	H
L	↑	⎍	⎏
↓	H	⎍	⎏



H = High level (steady state), L = Low level (steady state), ↑ = Transition from low to high level, ↓ = Transition from high to low level, ⎍ = One high-level pulse, ⎏ = One low-level pulse, X = Irrelevant (any input, including transitions)

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Figure A-1 74123 Retriggerable Monostable Multivibrator (One-Shot)

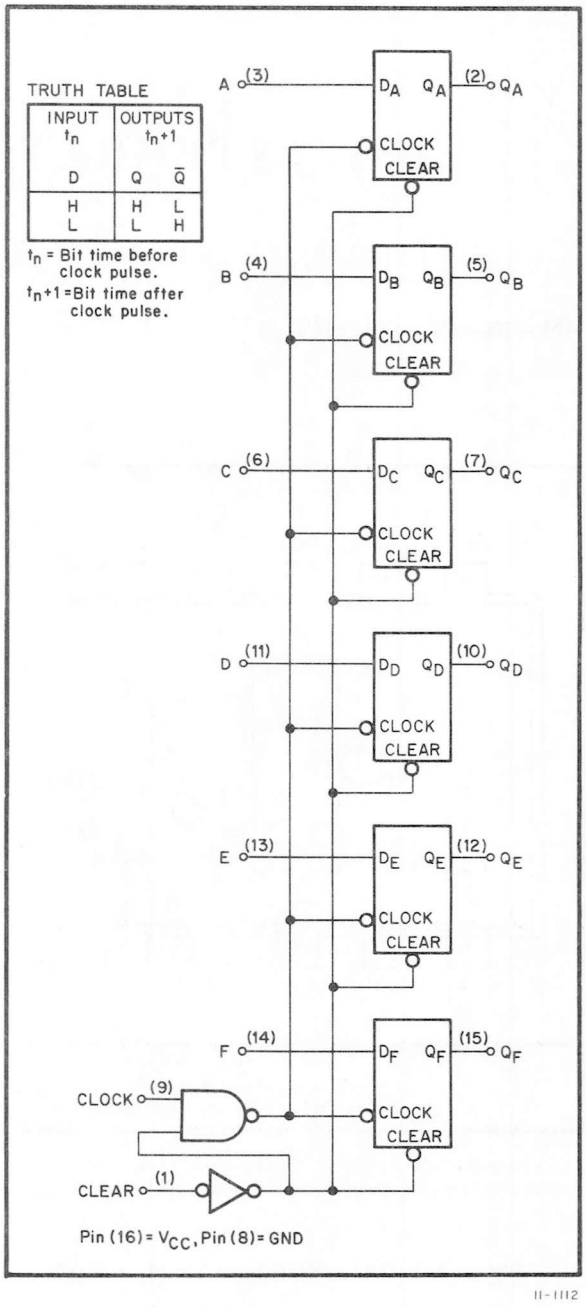

Figure A-2 74174 Quad D-Type Flip-Flops with Clear

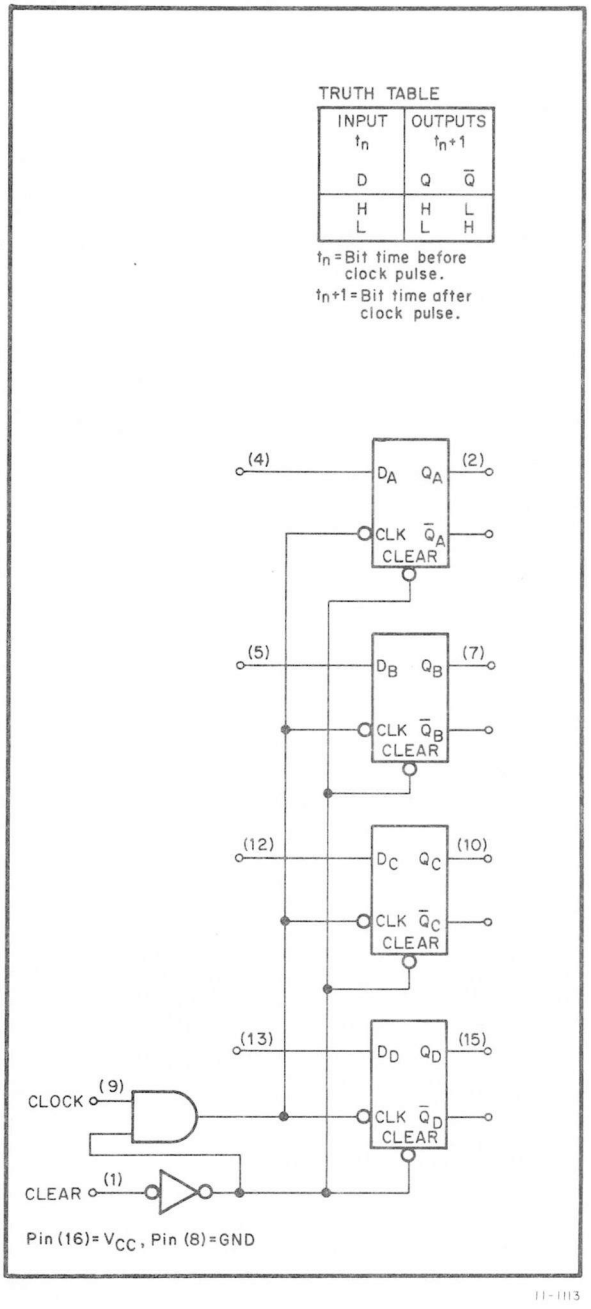

Figure A-3 74175 Quad D-Type Flip-Flops with Clear

APPENDIX B
ASCII CHARACTER CODES

Table B-1 list the ASCII character codes that are used by the LS11. Figure B-1 show an example of how the code for the character "F" would be contained in the LSDB.

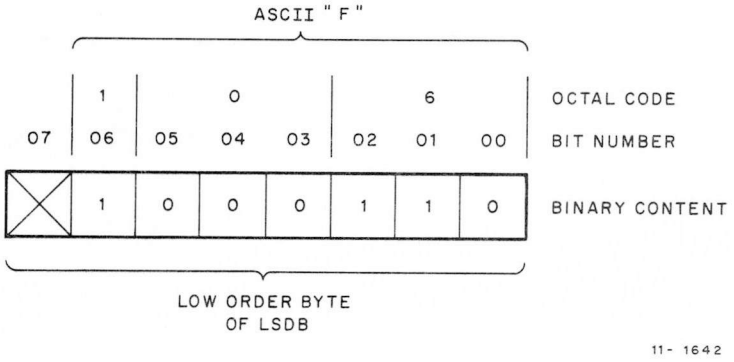

Figure B-1 Example of Character Format
for ASCII Character "F"

Table B-1
ASCII Character Set

7-Bit Octal Code	Character	Remarks
000	NUL	Null, Tape Feed
001	SOH	Start of Heading; also SOM, Start of Message
002	STX	Start of Text; also EOA, End of Address
003	ETX	End of Text; also EOM, End of Message
004	EOT	End of Transmission (END); shuts off TWX Machines
005	ENQ	Enquiry (ENQRY); also WRU
006	ACK	Acknowledge; also RU
*007	BEL	Rings the Bell
010	BS	Backspace; also FEO, Format Effector. Backspaces some Machines
011	HT	Horizontal Tab
*012	LF	Line Feed or Line Space (New Line); Advances Paper to Next Line
*013	VT	Vertical Tab (VTAB)
*014	FF	Form Feed to Top of Next Page (PAGE)
*015	CR	Carriage Return to Beginning of Line
*016	ELONG	Elongate, Doubles Size of Horizontal Printing Axis
017	SI	Shift In; Changes Ribbon Color to Black
020	DLE	Data Link Escape
*021	DC1	Device Control 1, Turns Transmitter (READER) On
022	DC2	Device Control 2, Turns Punch or Auxiliary On
*023	DC3	Device Control 3, Turns Transmitter (READER) Off
024	DC4	Device Control 4, Turns Punch or Auxiliary Off
025	NAK	Negative Acknowledge; also ERR, Error
026	SYN	Synchronous Idle (SYNC)
027	ETB	End of Transmission Block; also LEM, Logical End of Medium
030	CAN	Cancel (CANCL)
031	EM	End of Medium
032	SUB	Substitute
033	ESC	Escape
034	FS	File Separator
035	GS	Group Separator
036	RS	Record Separator
037	US	Unit Separator
040	SP	Space
041	!	
042	"	
043	#	
044	$	
045	%	
046	&	

* Commands used by LS11

Table B-1 (Cont)
ASCII Character Set

7-Bit Octal Code	Character	Remarks
047	'	Accent Acute or Apostrophe
050	(	
051	)	
052	*	
053	+	
054	,	
055	-	
056	.	
057	/	
060	0	
061	1	
062	2	
063	3	
064	4	
065	5	
066	6	
067	7	
070	8	
071	9	
072	:	
073	;	
074	<	
075	=	
076	>	
077	?	
100	@	
101	A	
102	B	
103	C	
104	D	
105	E	
106	F	
107	G	
110	H	
111	I	
112	J	
113	K	
114	L	
115	M	
116	N	
117	O	
120	P	
121	Q	
122	R	

Table B-1 (Cont)
ASCII Character Set

7-Bit Octal Code	Character	Remarks
123	S	
124	T	
125	U	
126	V	
127	W	
130	X	
131	Y	
132	Z	
133	[	
134	\	
135	]	
136	↑	
137	←	
140	`	Accent Grave
175	}	This Code Generated by Alt Mode
176	~	This Code Generated by ESC Key (If Present)
*177	DEL	Delete, Rub Out
		Lower Case Alphabet Follows
141	a	
142	b	
143	c	
144	d	
145	e	
146	f	
147	g	
150	h	
151	i	
152	j	
153	k	
154	l	
155	m	
156	n	
157	o	
160	p	
161	q	
162	r	
163	s	
164	t	
165	u	
166	v	
167	w	
170	x	
171	y	
172	z	
173	{	
174	|	

* Commands used by LS11

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DEC-11-HLSAA-A-D

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